



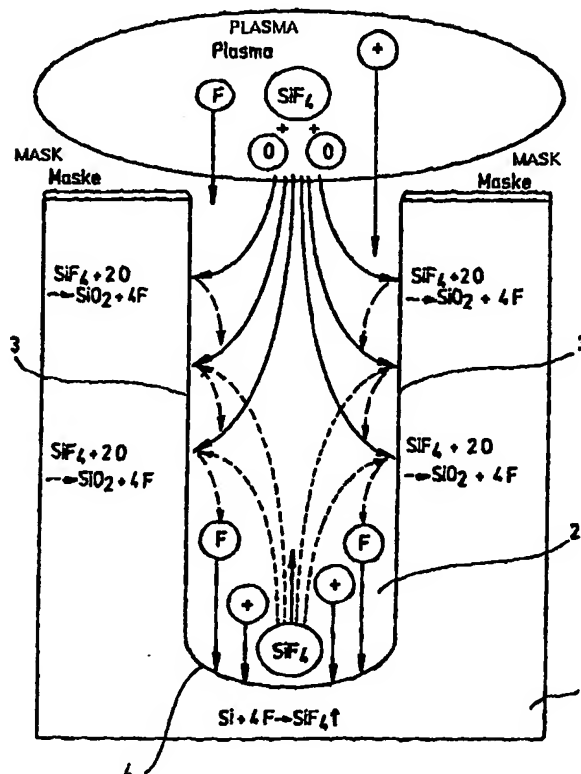
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PCT/DE98/00421 Februar 1998 (13.02.98)  1 (20.02.97) DE  Anspruch US): ROBERT 30 02 20, D-70442  Herr, Franz [DE/DE]; Dr. SCHILP, Andrea 71434 Schwäbisch Gmünd		(81) Bestimmungsstaaten: JP, KR, US, europäisches Patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  Veröffentlicht Mit internationalem Recherchenbericht.

# SELECTED PLASMA ETCHING METHOD FOR SILICON

## SELEKTIERTES PLASMAÄTZVERFAHREN FÜR SILICIUM

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**PCT**WELTORGANISATION FÜR GEISTIGES EIGENTUM  
Internationales BüroINTERNATIONALE ANMELDUNG VERÖFFENTLICHT NACH DEM VERTRAG ÜBER DIE  
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<b>(51) Internationale Patentklassifikation <sup>7</sup> :</b> <b>B81B 3/00</b>	<b>A1</b>	<b>(11) Internationale Veröffentlichungsnummer: WO 00/23376</b> <b>(43) Internationales Veröffentlichungsdatum:</b> 27. April 2000 (27.04.00)
<b>(21) Internationales Aktenzeichen:</b> PCT/DE99/03018 <b>(22) Internationales Anmeldedatum:</b> 22. September 1999 (22.09.99) <b>(30) Prioritätsdaten:</b> 198 47 455.5      15. Oktober 1998 (15.10.98)      DE <b>(71) Anmelder (für alle Bestimmungsstaaten ausser US):</b> ROBERT BOSCH GMBH [DE/DE]; Postfach 30 02 20, D-70442 Stuttgart (DE). <b>(72) Erfinder; und</b> <b>(75) Erfinder/Anmelder (nur für US):</b> BECKER, Volker [DE/DE]; Im Wiesele 7, D-76359 Marxzell (DE). LAERMER, Franz [DE/DE]; Witikoweg 9, D-70437 Stuttgart (DE). SCHILP, Andrea [DE/DE]; Seelenbachweg 15, D-73525 Schwabisch Gmuend (DE).		<b>(81) Bestimmungsstaaten:</b> JP, US, europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  <b>Veröffentlicht</b> <i>Mit internationalem Recherchenbericht. Vor Ablauf der für Änderungen der Ansprüche zugelassenen Frist; Veröffentlichung wird wiederholt falls Änderungen eintreffen.</i>
<b>(54) Title:</b> METHOD FOR PROCESSING SILICON USING ETCHING PROCESSES <b>(54) Bezeichnung:</b> VERFAHREN ZUR BEARBEITUNG VON SILIZIUM MITTELS ÄTZPROZESSEN <div data-bbox="511 1192 1140 1522"><p>The diagram is a cross-sectional view of a semiconductor structure. It shows a substrate (17) with a first silicon layer (15) on top. A barrier layer (12, 14, 16) is buried between the first silicon layer (15) and the substrate (17). The barrier layer consists of a central layer (12) and side layers (14, 16). Lateral recesses (21) are defined in the first silicon layer (15) by an etching mask (10). The recesses (21) are shown in cross-section as V-shaped or U-shaped structures. The barrier layer (12, 14, 16) is etched through in the exposed areas (23, 23') using a simplified process which is fully compatible with the process steps in IC integration technology. The diagram also shows a second silicon layer (17) and a third silicon layer (17'). The etching process (17) is shown as a series of steps, with the first step (17) and the second step (23, 23') being the most prominent. The etching process (17) is shown as a series of steps, with the first step (17) and the second step (23, 23') being the most prominent. The etching process (17) is shown as a series of steps, with the first step (17) and the second step (23, 23') being the most prominent.</p></div>		
<b>(57) Abstract</b> <p>The invention relates to a method for etching a first silicon layer (15) which is provided with an etching mask (10) for defining lateral recesses (21). Trenches (21') are produced in the area of the lateral recesses (21) in a first plasma etching process by means of anisotropic etching. As soon as a barrier layer (12, 14, 16) buried between the first silicon layer (15) and another silicon layer (17) is reached, the first etching process virtually comes to a stop (17). This barrier layer is then etched through in the exposed areas (23, 23') using a second etching process. An etching of the other silicon layer (17, 17') is then effected in a subsequent third etching process. This enables the production of free-standing structures for sensor elements using a simplified process which is fully compatible with the process steps in IC integration technology.</p>		



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(54) Electrostatic actuator

(57) An electrostatic actuator (10) comprises a first member (14) and a second member (12), the first member having a first opposed surface (15) that includes an array (17) of driven electrodes with pitch  $p_r$ , and the second member having a second opposed surface (13) and including an array (11) of drive electrodes. A support (e. g., 120) positions the first member adjacent the second member with the first opposed surface spaced apart from the second opposed surface by a spacing  $d$ . The ratio of the spacing and the pitch should be less than

eight, and is preferably less than 2.25. The support permits the first member to move relative to the second member, or vice versa. A voltage source (58,60) establishes a spatially substantially alternating voltage pattern on the array of driven electrodes. An electrode control (30) establishes a substantially alternating voltage pattern on the array of drive electrode, and selectively imposes a local disruption on the substantially alternating voltage pattern on the array of drive electrodes to move the movable one of the first member and the second member relative to the other.

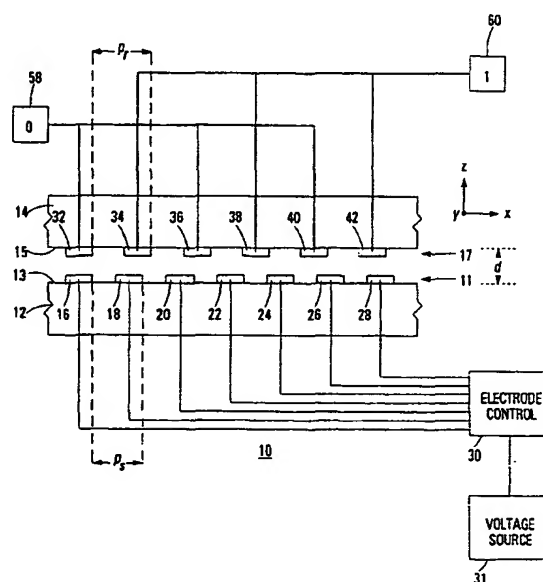


FIG.1

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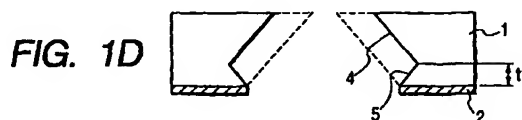
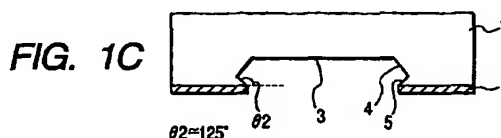
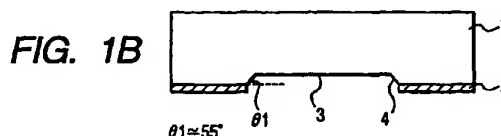
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(30) Priority: **20.06.1997 JP 164499/97**

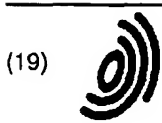
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(54) **A through hole formation method and a substrate provided with a through hole**

(57) A method of Si anisotropic etching makes it possible to relax the restrictions imposed upon the processing configuration of an Si substrate provided with the (100) plane orientation. This Si anisotropic etching method can be preferably used for the formation of the ink supply opening of an ink jet head, for example. When an Si material (Si substrate) having the (100) crystal plane orientation is processed by this anisotropic etching method, it is arranged to give heat treatment to such Si material in advance before etching. Thus, the processed section can be obtained in a bent configuration formed by the two (111) planes of crystal plane orientation. Therefore, the etching initiation surface is made smaller than that needed for the conventional art even when the same width should be obtained for a penetrating process, hence making a chip smaller accordingly for the reduction of costs.



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G11B 17/00

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(54) System and method for forming electrostatically actuated data storage mechanisms

(57) A plurality of data storage media (71) are integrated into a microfabricated data storage system (21). The media (71) are supported by a plurality of flexures (82) that allows the media (71) to move within a plane so that data can be stored at different locations on the media (71). The flexures (82), however, significantly resist any motion of the media (71) out of the plane. Therefore, tips (52) or other devices for writing or reading to or from the media (71) can be placed a small distance from the media (71), thereby facilitating attempts to microfabricate the data storage system (21). After forming the media (71) on a microfabricated wafer (32), the wafer (32) can be bonded to another microfabricated wafer (25), and the resulting structure can thereby be sealed by a gasket (62) in order to seal the media (71) within the data storage system (21). Preferably the bonding process to join the microfabricated wafers (25, 32) is CMOS (complementary metal-oxide semiconductor) compatible by using elements such as palladium and silicon that bond at relatively low temperatures.

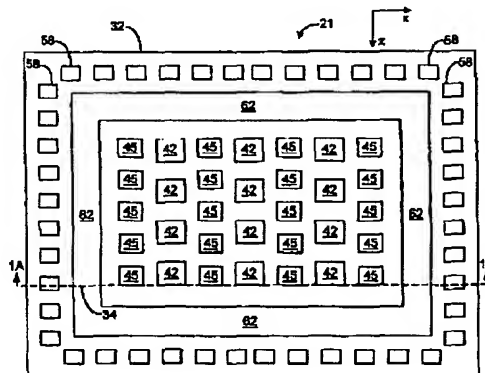


Fig. 1B

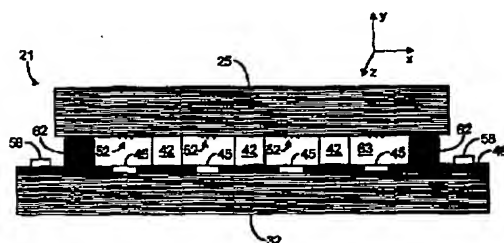


Fig. 1A

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